IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Poff et al.
Serial Number: 09/886,167
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Docket No.: IREA0002C
Group Art Unit: 2171
Examiner: Unassigned
Title: HARDWARE ACCELERATOR FOR AN OBJECT-ORIENTED PROGRAMMING LANGUAGE

September 12, 2001

Commissioner of Patents and Trademarks
Washington, DC 20231

Preliminary Amendment

Sir:

Please add the following amendment and remarks.
Please charge the new claim fees to deposit account no. 07-1445.

In the Claims:

41. (new) An apparatus for accelerating a processor running an object-oriented programming language, comprising:

a hardware accelerator interfaced with said processor for implementing at least one application framework of said object-oriented programming language, wherein said at least one application framework comprises a set of classes that embodies an abstract design for solutions to a number of related problems; and

a means for a software stub that controls interfacing of said hardware accelerator with said processor.

42. (new) The apparatus of Claim 41, further comprising a hardware object management system interacting with said hardware accelerator for managing instances of said application framework and the states of values assigned to said instances based upon said hardware object management system interacting with said hardware accelerator circuit.

43. (new) The apparatus of Claim 41, wherein said hardware accelerator comprises:

an Input/Output request queue interacting with said processor for receiving and sequentially storing said instructions pending execution of each instruction;

a task processor for processing said instructions from said Input/Output request queue; and

a means for an active object list for tracking the number of reference counts to an instance and for deallocating an instance that is not in use based upon a result of said task processor processing said instructions.

44. (new) The apparatus of Claim 41, wherein said object-oriented programming language is C++.

45. (new) The apparatus of Claim 41, wherein said object-oriented programming language is Java.

46. (new) An apparatus for accelerating a processor running the Java programming language, comprising:

a hardware accelerator for implementing at least one Java application framework, wherein said at least one Java application framework comprises a set of classes that embodies an abstract design for solutions to a number of related problems;

a hardware object management system communicatively interfaced with said processor for managing instances of application framework and the states of values assigned to said instances, said hardware object management system comprising

an Input/Output request queue for receiving and sequentially storing said instructions pending execution of each instruction through communication across said communication interface with said processor,

a task processor for processing said instructions received from said Input/Output request queue through interaction with said hardware accelerator, and

a means for an active object list for tracking the number of reference counts to an instance and for deallocating an instance that is not in use based upon said task processor interaction with said hardware accelerator; and

a means for a software stub to control of interfacing said hardware object management system with said processor.

47. (new) The apparatus of Claim 46, wherein said hardware accelerator further comprising a Java.AWT circuit implementing the Java.AWT application framework through interactions with said hardware object management system.

48. (new) The apparatus of Claim 47,

wherein said Java.AWT circuit is further comprised of

a windowing/view system communicating with said hardware object management system and interacting with a rendering engine.

49. (new) The apparatus of Claim 48, wherein said windowing/view system comprises:

a general graphics controller communicating with said hardware object management system and communicating with said rendering engine for creating frames and components and for passing data to said rendering engine;

a means for a window manager communicating with said general graphics controller for managing said frames;

a means for a layout manager communicating with said general graphics controller for managing container hierarchies within said frame; and

a means for a component manager communicating with said general graphics controller for managing component hierarchies within said container.

50. (new) The apparatus of Claim 46, wherein said hardware accelerator further comprising a Java.NET circuit communicating with said hardware object management system implementing the Java.NET and Java.IO application

frameworks through communication with said hardware object management system.

51. (new) The apparatus of Claim 50, wherein said Java.NET circuit further comprising:

a windowing/view system communicating with said task processor and communicating with a connectivity engine.

52. (new) The apparatus of Claim 51, wherein said windowing/view system comprises:

a network controller responsive to said hardware object management system, said network controller executing microcode to implement Java.NET framework equivalencies, wherein said network controller operates as an abstraction layer over protocols supported by said connectivity engine through communicating with said connectivity engine;

a means for a network query mechanism for performing DNS lookups and for reporting results to said network controller through communicating with said network controller;

a means for a socket manager for managing sockets in use by applications through communicating with said network controller; and

a means for a stream manager for shuttling input and output data through a link supported by said protocols through communicating with said network controller.

53. The apparatus of Claim 46, wherein said hardware accelerator is formed as a part of an application specific integrated circuit.

54. (new) An apparatus for accelerating a processor running an object-oriented programming language, comprising:

a hardware accelerator interfaced with said processor for implementing at least one application framework of said object-oriented programming language, wherein said at least one application framework comprises a set of classes further comprising:

an Input/Output request queue interacting with said processor for receiving and sequentially storing said instructions pending execution of each instruction;

a task processor for processing said instructions from said Input/Output request queue; and

a means for an active object list for tracking the number of reference counts to an instance and for deallocating an instance that is not in use based upon a result of said task processor processing said instructions;

a hardware object management system interacting with said hardware accelerator for managing instances of said application framework and the states of values assigned to said instances based upon said hardware object management system interacting with said hardware accelerator circuit; and

a means for a software stub that controls interfacing of said hardware accelerator with said processor.

55. (new) The apparatus of Claim 54, wherein said hardware accelerator further comprises a Java.AWT circuit interacting with said task processor to implement the Java.AWT application framework through interactions with said task processor.

56. (new) The apparatus of Claim 55,

wherein said Java.AWT circuit is further comprised of

a windowing/view system communicating with said task processor and interacting with a rendering engine.

57. (new) The apparatus of Claim 56, wherein said windowing/view system comprises:

a general graphics controller communicating with said task processor and interacting with said rendering engine for creating frames and components and for passing data to said rendering engine;

a window manager communicating with said general graphics controller for managing said frames;

a layout manager communicating with said general graphics controller for managing container hierarchies within said frame; and

a component manager communicating with said general graphics controller for managing component hierarchies within said container.

58. (new) The apparatus of Claim 54, wherein said hardware accelerator implements the Java.NET and Java.IO application frameworks.

59. (new) The apparatus of Claim 58, further comprising:

a windowing/view system communicating with said task processor and interacting with a connectivity engine.

60. (new) The apparatus of Claim 59, wherein said windowing/view system comprises:

a network controller responsive to said hardware object management system, said network controller executes microcode to implement Java.NET framework equivalencies, wherein said network controller operates as an abstraction layer over protocols supported by said connectivity engine through interactions between said network controller and said connectivity engine;

a network query mechanism for performing DNS lookups and for reporting results to said network controller through said network query mechanism interacting with said network controller;

a socket manager for managing sockets in use by applications through interactions between said socket manager and said network controller; and

a stream manager for shuttling input and output data through a link supported by said protocols by interactions between said stream manager and said network controller.

61. (new) The apparatus of Claim 54, wherein said hardware accelerator is formed as a part of an application specific integrated circuit.

62. (new) The apparatus of Claim 54, wherein said object-oriented programming language is Java.

63. (new) The apparatus of Claim 54, wherein said object-oriented programming language is C++.

Remarks

These claims are being added to further clarify the invention and do not constitute new matter.

The Applicants respectfully request that all Claims in this continuation application be allowed for at least the reasons stated in previous responses for the claims of the parent patent application, which is in condition for allowance, as well as the reasons stated in the response filed with this patent application.

Respectfully Submitted,

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